



# iPROVE

## SCE-MI Coemulation

### Overview

iPROVE SCE-MI Coemulation Package provides an easy of use design flow for co-running synthesized hardware blocks with C-based transaction-level verification environment.

iPROVE is a design verification tool that verifies DUT (Design Under Test) by mapping into FPGA. Thus, iPROVE helps designers to verify their designs prior to fabrication in silicon.

iPROVE tool set consists of hardware and software; iPROVE hardware is a PCI card and iPROVE software includes device driver for various platforms, a set of API/PLI/VPI/FLI/VHPI libraries and GUI based design environment. iPROVE provides BILA (Built-In Logic Analyzer) which monitors signals of DUT with various triggering conditions. iPROVE also provides DPP (Data Pumping Port) through which the external hardware can be connected to.



### Coemulation Highlights

- **SCE-MI Version 1.1 supported**
- **Automatic generation of SCE-MI infrastructure through scemilinker™**
- **iPROVE/SCE-MI co-simulation supported – software only simulation using industry standard Verilog-HDL simulators prior to co-emulation**
- **Built-in-logic analyzer™ supported to monitor pin and net signals**
- **C/C++ and SystemC environment supported**
- **Various platforms supported:** PC Linux RedHat, Sun Solaris
- **Industry standard compilers supported:** GNU GCC

### iPROVE Features

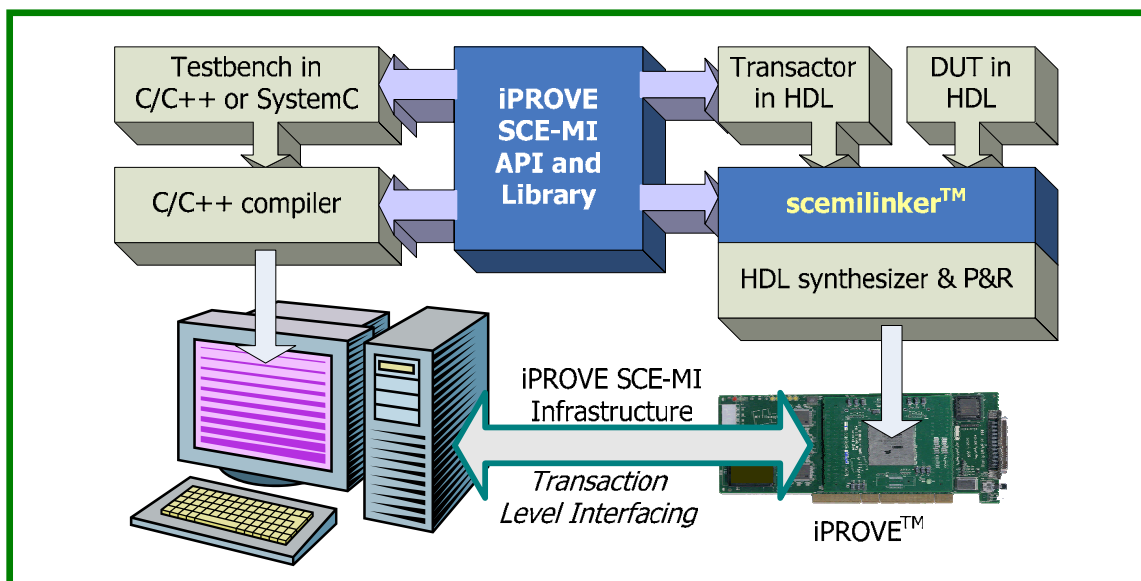
#### Hardware

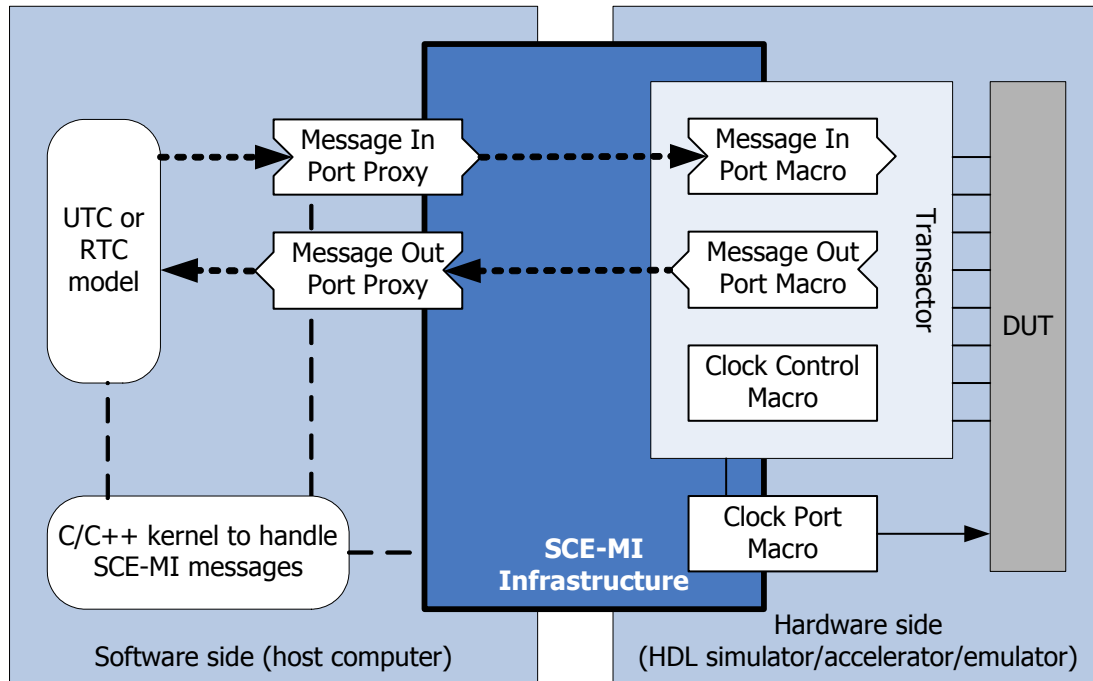
- PCI controller block for 66MHz/33MHz, 64bit/32bit with DMA capability
- BILA for hardware debugging
- On-board memory
- DPP as an external interfacing port
- Xilinx Virtex II / Virtex 4 support
- Reconfiguration through PCI

#### Software

- Device drivers for various platforms
- Various APIs for C/C++ and Verilog/VHDL co-simulation or testing
- FPGA netlist builder for Xilinx/Altera
- Supporting cycle-level and transaction-based verification modes

iPROVE SCE-MI Coemulation package provides a transaction-level verification environment where user's design block mapped on FPGA can be emulated/simulated using high-level language.





## High-level view of SCE-API/MI

### SCE-API/MI

The SCE-API/MI (Standard Co-Emulation API – Modeling Interface), provided by Accellera ITC (Interface Technical Committee, [www.eda.org/itc](http://www.eda.org/itc)), defines a high-speed, asynchronous, transaction-level interface between simulator or testbenches and hardware-assisted solutions such as emulator, accelerator, or rapid prototypes.

The SCE-MI provides a message-passing environment in which message channels run between the software side and the hardware side. The software side means UTC (Un-Timed C) or RTC (Register Transfer level C) models running on the host computer and the hardware side means any simulator capable of executing RTL or gate-level models.

### Deliverables

- **Prerequisites**
  - ▶ **iPROVE system** including iPROVE hardware and software
  - ▶ **New iPROVE software:** iPROVE SCE-MI Coemulation feature added iPROVE software version 4.0.
- **New license feature:** iPROVE SCE-MI Coemulation feature added
- **Documentation:** iPROVE SCE-MI Coemulation Manual

• **H.Q.:** Dynalith Systems Co., Ltd.  
2nd Fl. Taejin Building,  
14-2 Yangjae-Dong Seocho-Gu,  
Seoul, 137-888, Korea  
Tel: +82-2-556-0020  
Fax: +82-2-556-2252

• **R&D Center:**  
373-1 Guseong-Dong, Yuseong-Gu  
CHiPS B/D 3rd Fl., KAIST,  
Daejeon 305-701, Korea  
Tel: +82-42-862-6411  
Fax: +82-42-862-6410

• **USA Office:** Dynalith Systems, Inc.  
10130 Firwood Dr., Cupertino,  
CA 95054, USA  
Tel: +1-408-517-8917  
Fax: +1-408-517-8917

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**Web: [www.dynalith.com](http://www.dynalith.com)**

**E-mail: [info@dynalith.com](mailto:info@dynalith.com)**