



iSAVE-MP

SoC Design Platform

Overview

Dynalith Systems' new product, iSAVE-MP, provides a seamless design platform for HW/SW co-design and co-verification for System-on-a-Chip (SoC).

Designers can verify their ASIC or SoC design from the architecture level to the register-transfer level (RTL) using iSAVE-MP, which supports multiple languages (C/C++, SystemC, HDL, and EDIF) and mixed levels (behavioral to cycle-level).

iSAVE-MP's hardware utilizes multi-processor architecture to provide scalable computing power, multiple Split Target interface ARchitectures (STARs) to provide scalable target interfaces, and Reconfigurable FPGA Engine (RFE) modules to support HDL design. Embedded system design using processor cores, such as ARM and DSP cores, are supported.

iSAVE-MP provides easy-to-use verification environment using Linux-based stand alone system. iSAVE-MP is easily incorporated with existing design blocks described either in HDL or in EDIF. Moreover, iSAVE-MP has various options to extend design and verification environments such as C-based design, in-system verification and embedded core design.

Designer can choose a transaction-based mode for fast verification and a cycle-based mode for signal-level verification using iSAVE-MP.

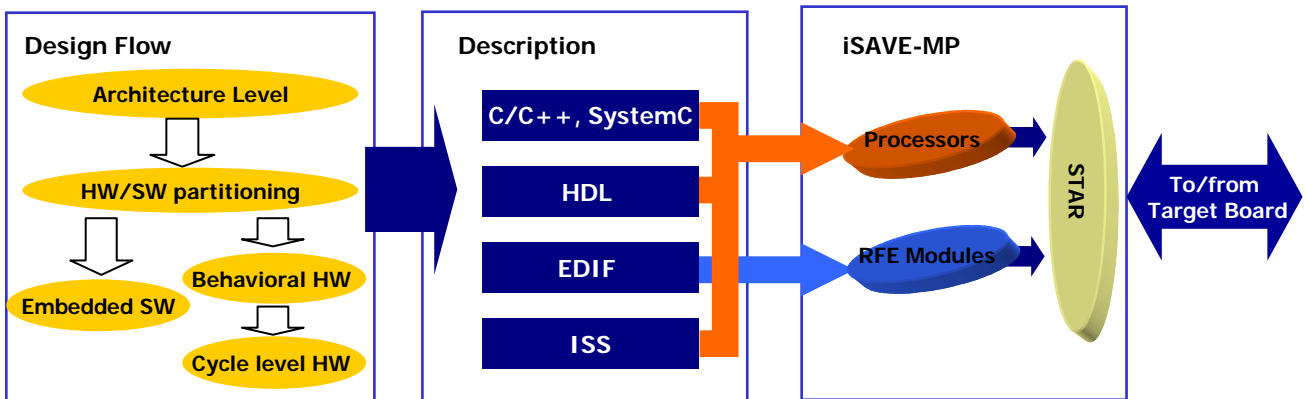
It also provides various debugging features for an easy development environment. These features include a source level debugger, Pin Signal Analyzer (PSA) and Software Variable Analyzer (SVA).

iSAVE-MP Features

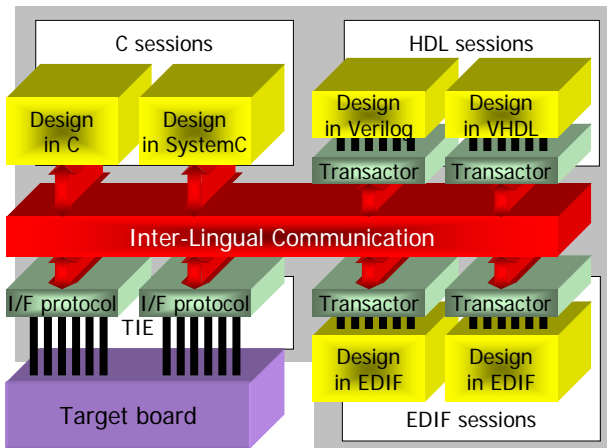
- Powerful processing engine
 - Linux-based stand-alone solution
 - Scalable computing power with multi-processor architecture
 - Scalable target interfacing capabilities with multiple STARs
- Multiple language verification
 - C/C++, SystemC, Verilog, VHDL, EDIF
 - HDL design supported directly with RFE modules
- Multiple verification mode
 - Transaction-based mode for fast verification
 - Cycle-level mode for signal level verification
- Powerful debugging capabilities
 - Pin Signal Analyzer (PSA) , a built-in logic analyzer with triggering support, enables the user to monitor the pin signals
 - Software Variable Analyzer (SVA) enables tracing software variables
 - GNU DeBugger (GDB)-based debugger for software debugging
- Easy-to-use graphical user interface
- In-system verification



iSAVE-MP supports the design flow from architecture level to Register Transfer Level (RTL).



iSAVE-MP Structure



iSAVE-MP utilizes the Inter-Lingual Communication (ILC) technology so that design blocks represented/implemented in different description languages can communicate with each other.

Using ILC, iSAVE-MP supports multiple languages and multiple abstraction levels effectively.

Also, the special structure of STAR enables designers to connect to a large number of I/O pins on a target board.

Therefore, iSAVE-MP provides the optimized SoC design platform that supports a seamless design flow from architecture level to RTL level.

Overall Specification

Computing power	
Number of processors	one or more*
Clock speed	1GHz or higher*
Target interface	
Num of IO pins per STAR	Up to 350 pins
Num STAR per system	Up to 3 STARs
IO driving technology	3.3V LVTTTL
IO driving speed	Up to 100MHz*
Number of IO pins to be monitored	Up to 384pins per STAR
RFE (FPGA module)	
Gate capacity	From 1M to 8M gates*

* Depending on configurations(Subject to change)

Required Third Party Information

- HDL Simulator: ModelSim (SE or PE)
- Lverifier: ModelSim (SE or PE)
or Cadence Verilog-XL
- Logic Synthesizer: Synopsys DC with FPGA Compiler, FPGA Compiler II, Synplicity Synplify, Synplify Pro, Mentor Graphics LeonardoSpectrum
- FPGA Mapper: Xilinx Alliance ISE (Windows or Solaris version)

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